

100

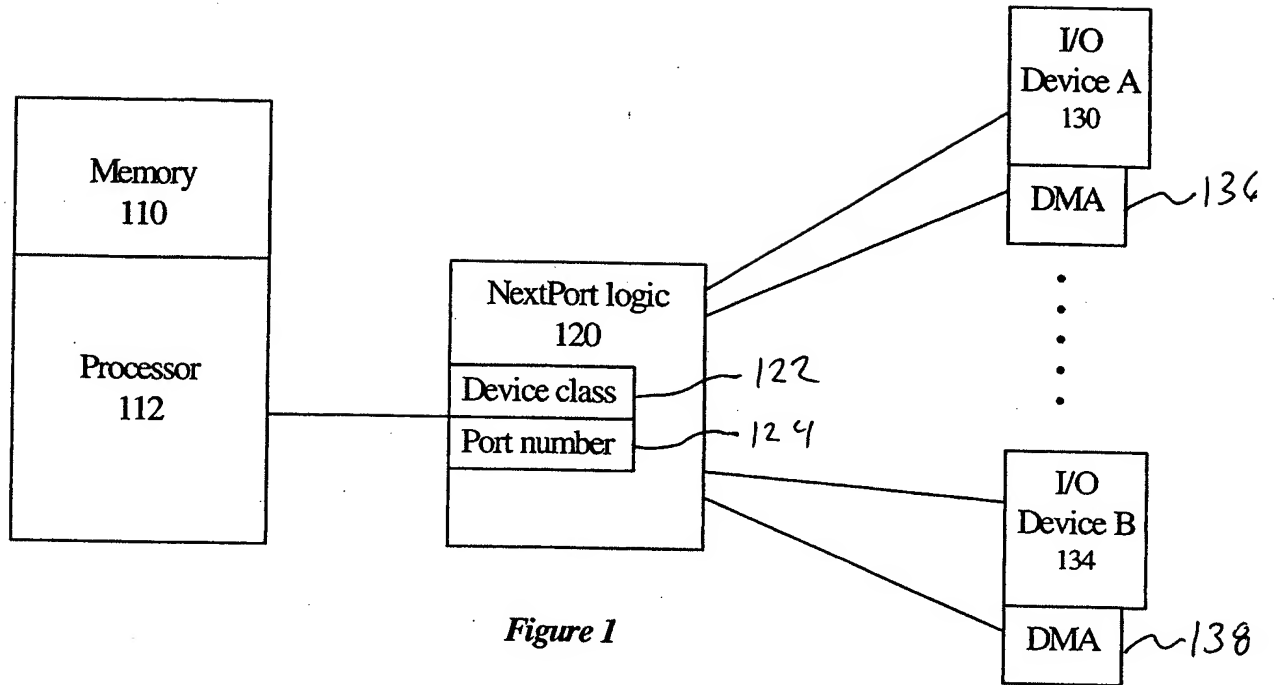


Figure 1

Table entry for Device A	Context pointer	Handler routine address
Table entry for Device A DMA	Context pointer	Handler routine address
Table entry for Device B	Context pointer	Handler routine address
Table entry for Device B DMA	Context pointer	Handler routine address
⋮	⋮	⋮

Figure 2

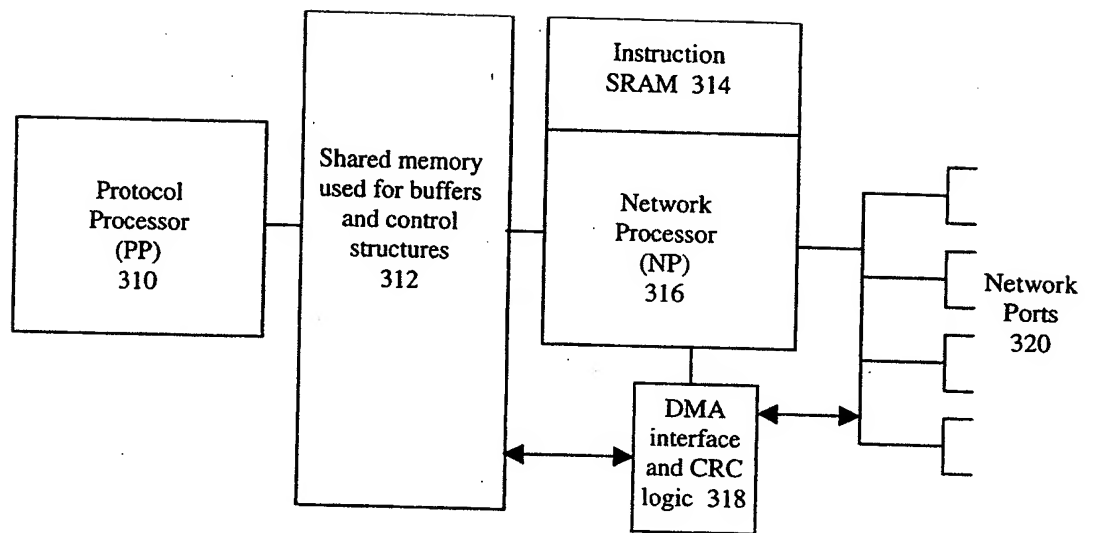


Figure 3

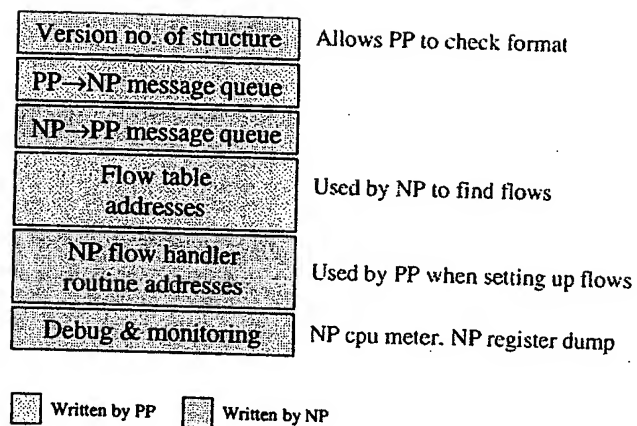


Figure 4

7 state variables (to be preloaded into registers) Used for current buffer pointers, cell counts, policing params, etc.
NP rx handler address
NP tx handler address
Current buffer
Buffer source and/or destination
Type, Flags
Local buffer queue (switch flows)
Other flow-specific data

First part has a similar format in all flows.
A flow is invoked by a single instruction:

- loads 8 or 9 registers
- jumps to handler routine

Figure 5

(These steps are interleaved with operations on other flows and ports)

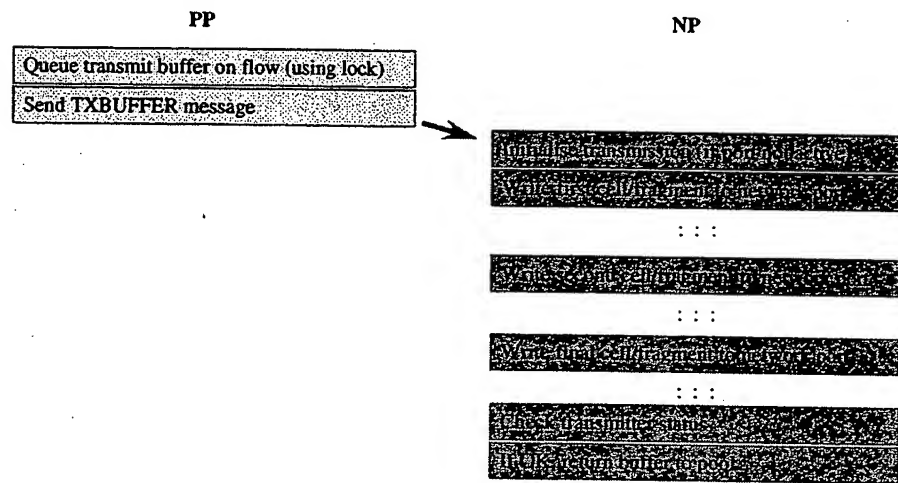


Figure 6

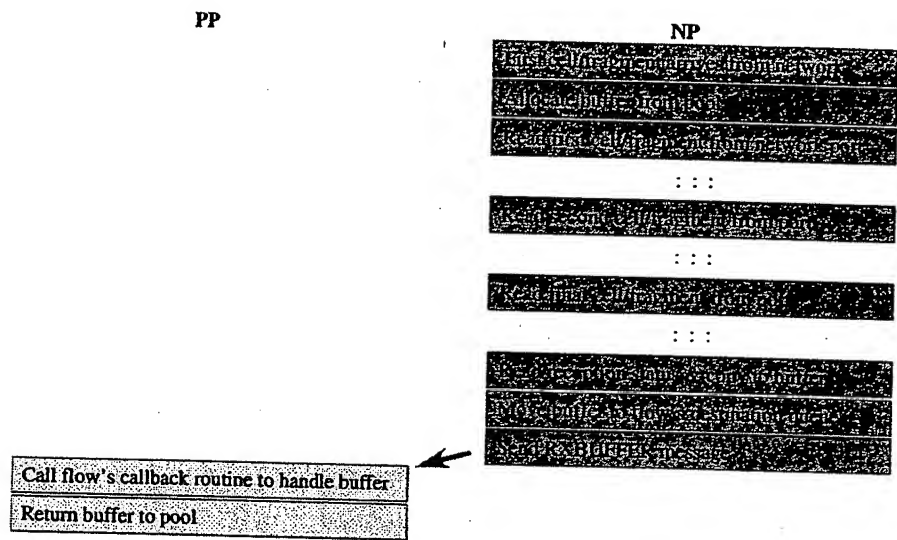


Figure 7

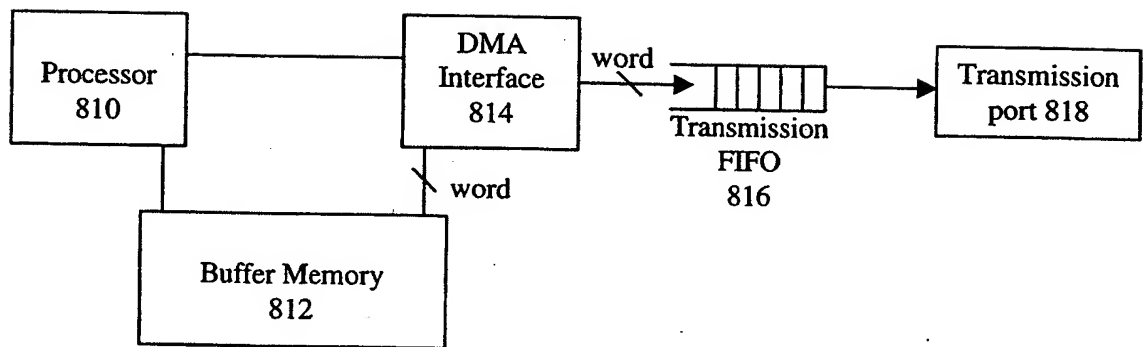


Figure 8

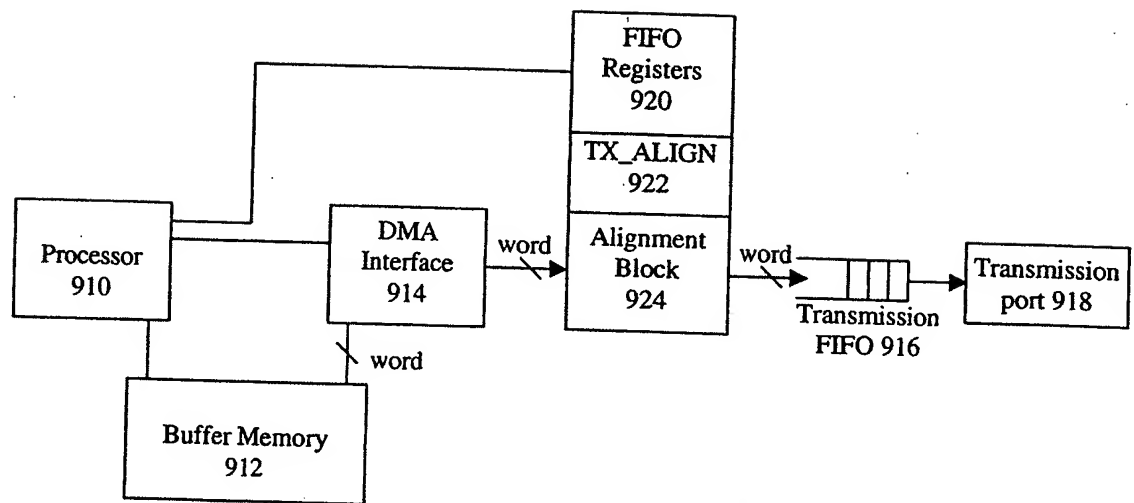


Figure 9

1000

OCTETS field in TX_ALIGN register	Least significant 2 bits of DMA address	KEEP_ ALIGN flag	TX_ALIGN register word at start	Next word from memory	TX_ALIGN register word after first memory cycle	Word written to FIFO
XX	00	0	XXXX.XXXX	pqrs.vwyz	XXXX.XX00	pqrs.vwyz
XX	01	0	XXXX.XXXX	pqrs.vwXX	pqrs.vw01	No write
XX	10	0	XXXX.XXXX	pqrs.XXXX	pqrs.XX02	No write
XX	11	0	XXXX.XXXX	pqXX.XXXX	pqXX.XX03	No write
00	00	1	XXXX.XX00	pqrs.vwyz	XXXX.XX00	pqrs.vwyz
00	01	1	XXXX.XX00	pqrs.vwXX	pqrs.vw01	No write
00	10	1	XXXX.XX00	pqrs.XXXX	pqrs.XX02	No write
00	11	1	XXXX.XX00	pqXX.XXXX	pqXX.XX03	No write
01	00	1	ghij.kl01	pqrs.vwyz	pqrs.vw01	yzgh.ijkl
01	01	1	ghij.kl01	pqrs.vwXX	pqrs.XX02	vwgh.ijkl
01	10	1	ghij.kl01	pqrs.XXXX	pqXX.XX03	rsgh.ijkl
01	11	1	ghij.kl01	pqXX.XXXX	XXXX.XX00	pggh.ijkl
10	00	1	ghij.XX02	pqrs.vwyz	pqrs.XX02	vwyz.ghij
10	01	1	ghij.XX02	pqrs.vwXX	pqXX.XX03	rsvw.ghij
10	10	1	ghij.XX02	pqrs.XXXX	XXXX.XX00	pqrs.ghij
10	11	1	ghij.XX02	pqXX.XXXX	pqgh.ij01	No write
11	00	1	ghXX.XX03	pqrs.vwyz	pqXX.XX03	rsvw.yzgh
11	01	1	ghXX.XX03	pqrs.vwXX	XXXX.XX00	pqrs.vwgh
11	10	1	ghXX.XX03	pqrs.XXXX	pqrs.gh01	No write
11	11	1	ghXX.XX03	pqXX.XXXX	pqgh.XX02	No write

Figure 10

1100

OCTETS field in TX_ALIGN register	TX_ALIGN register word at start	Word written to FIFO register	FIFO register written	TX_ALIGN after FIFO register write	Word written to FIFO
00	XXXX.XX00	pqrs.vwyz	TX FIFO0	XXXX.XX00	pqrs.vwyz
00	XXXX.XX00	XXrs.vwyz	TX FIFO1	rsvw.yz01	No write
00	XXXX.XX00	XXXX.vwyz	TX FIFO2	vwyz.XX02	No write
00	XXXX.XX00	XXXX.XXyz	TX FIFO3	yzXX.XX03	No write
01	ghij.kl01	pqrs.vwyz	TX FIFO0	pqrs.vw01	yzgh.ijkl
01	ghij.kl01	XXrs.vwyz	TX FIFO1	rsvw.XX02	yzgh.ijkl
01	ghij.kl01	XXXX.vwyz	TX FIFO2	vwXX.XX03	yzgh.ijkl
01	ghij.kl01	XXXX.XXyz	TX FIFO3	XXXX.XX00	yzgh.ijkl
10	ghij.XX02	pqrs.vwyz	TX FIFO0	pqrs.XX02	vwyz.ghij
10	ghij.XX02	XXrs.vwyz	TX FIFO1	rsXX.XX03	vwyz.ghij
10	ghij.XX02	XXXX.vwyz	TX FIFO2	XXXX.XX00	vwyz.ghij
10	ghij.XX02	XXXX.XXyz	TX FIFO3	pqgh.ij01	No write
11	ghXX.XX03	pqrs.vwyz	TX FIFO0	pqXX.XX03	rsvw.yzgh
11	ghXX.XX03	XXrs.vwyz	TX FIFO1	XXXX.XX00	rsvw.yxgh
11	ghXX.XX03	XXXX.vwyz	TX FIFO2	vwyz.gh01	No write
11	ghXX.XX03	XXXX.XXyz	TX FIFO3	yzgh.XX02	No write

Figure 11

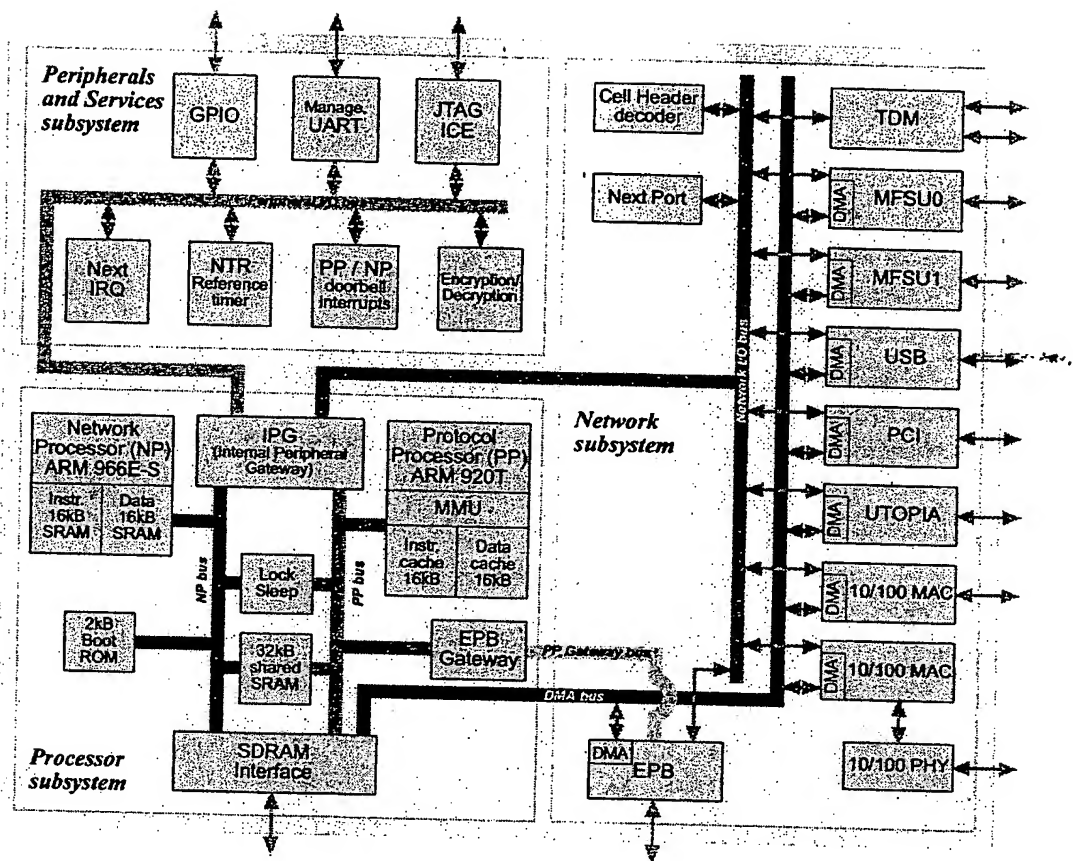


Figure 12

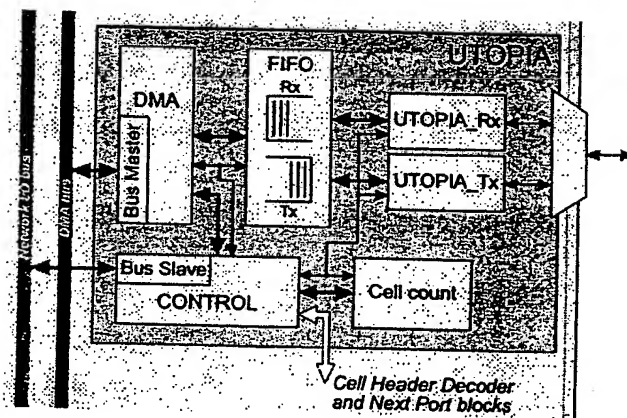


Figure 13

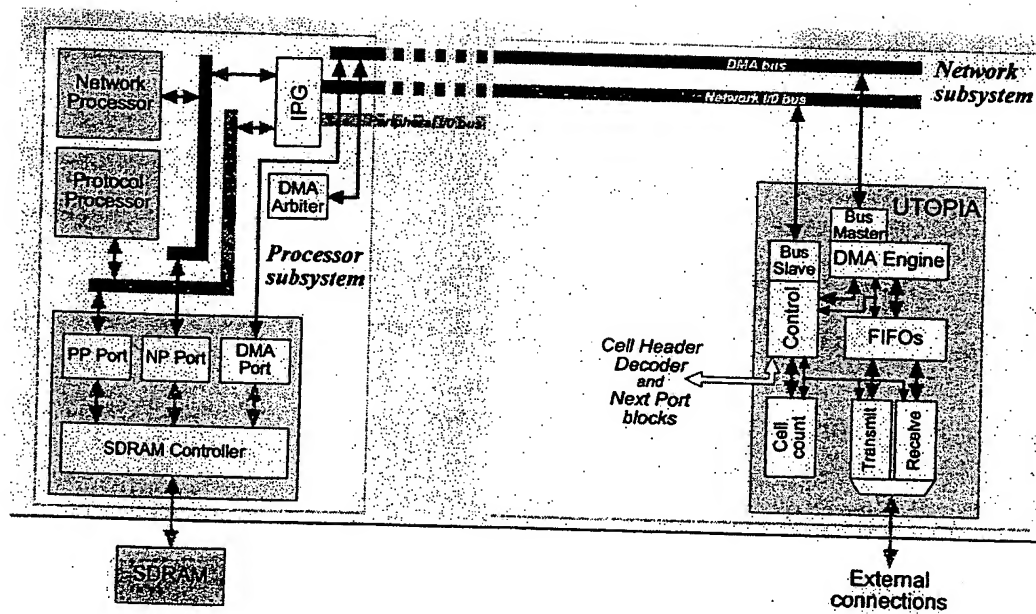


Figure 14

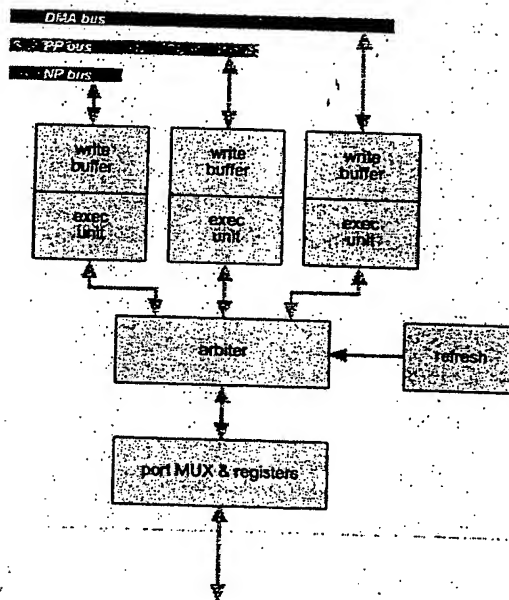


Figure 15

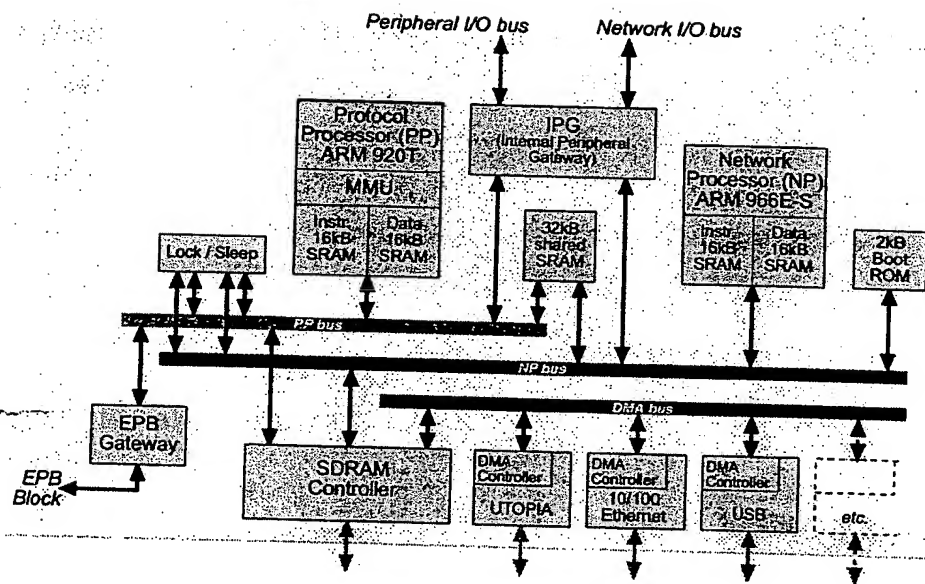


Figure 16

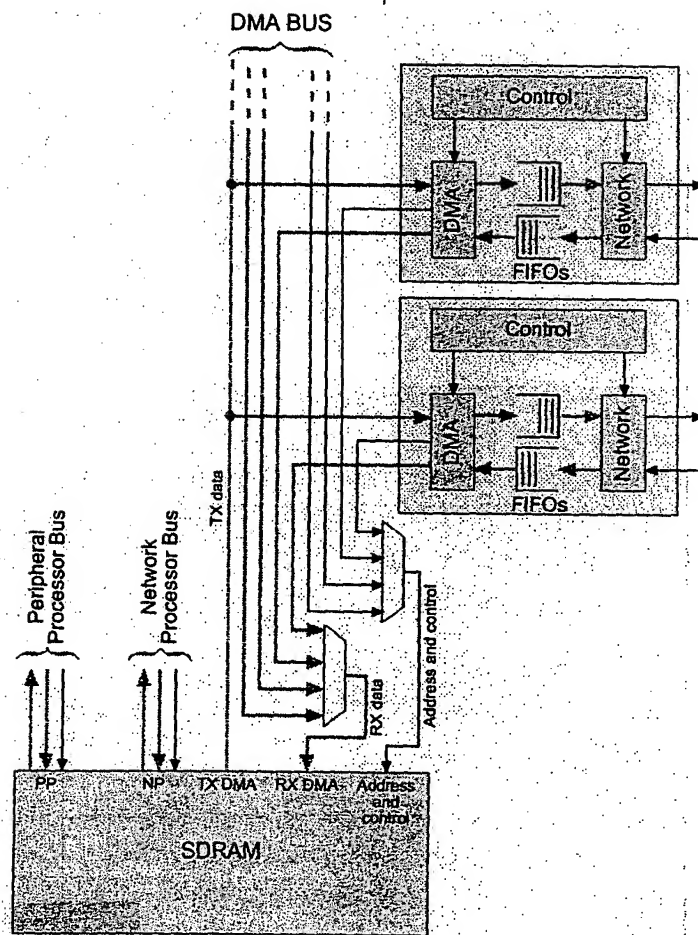


Figure 17